WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a first array of memory cells, each memory cell in the first array comprising a resistive element and a Schottky diode coupled in series and having first and second terminals;

a first plurality of bit lines, one bit line for each column of the first array, each bit line coupled to the first terminal of memory cells in a respective column of the first array; and

a first plurality of word lines, one word line for each row of the first array, each word line coupled to the second terminal of memory cells in a respective row of the first array.

2. The integrated circuit of claim 1, wherein the resistive element for each memory cell is formed by a film of a perovskite material.

3. The integrated circuit of claim 2, wherein the perovskite material is $Pr_{0.7}Ca_{0.3}MnO_3$.

4. The integrated circuit of claim 2, wherein the perovskite material is a colossal magnetoresistive (CMR) material.

5. The integrated circuit of claim 1, wherein the Schottky diode for each memory cell is formed by a thin film of amorphous silicon.

6. The integrated circuit of claim 1, wherein a memory cell is formed at each cross point between a bit line and a word line.

7. The integrated circuit of claim 1, wherein the resistive element for each memory cell is programmable to have one of two resistance states.

8. The integrated circuit of claim 1, further comprising:

a bit line driver operative to drive the first plurality of bit lines for reading and programming the memory cells.

9. The integrated circuit of claim 1, further comprising:

a word line decoder operative to drive the first plurality of word lines for reading and programming the memory cells.

10. The integrated circuit of claim 1, further comprising:

a plurality of sense amplifiers coupled to the first plurality of bit lines, each sense amplifier operative to sense a current on a respective bit line to determine a resistance state of a resistive element for a memory cell selected for reading.

11. The integrated circuit of claim 1, further comprising:

a second array of memory cells, each memory cell in the second array comprising a resistive element and a Schottky diode coupled in series and having first and second terminals;

a second plurality of bit lines, one bit line for each column of the second array, each bit line coupled to the first terminal of memory cells in a respective column of the second array; and

a second plurality of word lines, one word line for each row of the second array, each word line coupled to the second terminal of memory cells in a respective row of the second array.

12. A memory device comprising:

an array of memory cells, each memory cell comprising a resistive element and a Schottky diode coupled in series and having first and second terminals;

a plurality of bit lines, one bit line for each column of the array, each bit line coupled to the first terminal of memory cells in a respective column of the array;

a plurality of word lines, one word line for each row of the array, each word line coupled to the second terminal of memory cells in a respective row of the array;

a bit line driver operative to drive the plurality of bit lines for reading and programming the memory cells;

a word line decoder operative to drive the plurality of word lines for reading and programming the memory cells; and

a plurality of sense amplifiers coupled to the plurality of bit lines, each sense amplifier operative to sense a current on a respective bit line to determine a resistance state of a resistive element for a memory cell selected for reading.

13. The memory device of claim 12, wherein the resistive element for each memory cell is formed by a film of a perovskite material.

14. The memory device of claim 12, wherein the Schottky diode for each memory cell is formed by a thin film of amorphous silicon.

15. A method of fabricating a resistive memory, comprising:

forming a first plurality of word lines, one word line for each row of a first memory array;

forming a first plurality of memory cells for the first memory array, each memory cell comprising a film of a perovskite material for a resistive element and a thin film of amorphous silicon for a Schottky diode; and

forming a first plurality of bit lines, one bit line for each column of the first memory array, wherein each word line is coupled to a first terminal of memory cells in a respective row of the first memory array, and wherein each bit line is coupled to a second terminal of memory cells in a respective column of the first memory array.

16. The method of claim 15, wherein the perovskite material is $Pr_{0.7}Ca_{0.3}MnO_3$.

17. The method of claim 15, further comprising:

forming a second plurality of word lines, one word line for each row of a second memory array;

forming a second plurality of memory cells for the second memory array, each memory cell comprising a film of a perovskite material for a resistive element and a thin film of amorphous silicon for a Schottky diode; and

forming a second plurality of bit lines, one bit line for each column of the second memory array, wherein each word line is coupled to a first terminal of memory cells in a respective row of the second memory array, and wherein each bit line is coupled to a second terminal of memory cells in a respective column of the second memory array.

18. A method of reading a selected memory cell in a resistive memory comprising a plurality of memory cells, each memory cell including a resistive element and a Schottky diode coupled in series, the method comprising:

providing a reverse bias voltage across each memory cell not selected for reading;

providing a forward bias voltage across the selected memory cell; and

sensing a current from the selected memory cell to determine a resistance state of the resistive element for the selected memory cell.

19. A method of programming a selected memory cell in a resistive memory comprising a plurality of memory cells, each memory cell including a resistive element and a Schottky diode coupled in series , the method comprising:

providing a reverse bias voltage across each memory cell not selected for programming; and

providing one or more electric pulses with a forward bias voltage across the selected memory cell.

20. The method of claim 19, wherein the resistive element for the selected memory cell is programmed to a high resistance state with one or more electric pulses of a first amplitude and a first width and programmed to a low resistance state with one or more electric pulses of a second amplitude and a second width.

21. The method of claim 20, wherein the first amplitude is higher than the second amplitude and the first width is shorter than the second width.